

HX6572 Hall-Effect sensor, designed for electronic commutation of brush-less DC motor applications. The device includes an on-chip Hall voltage generator for magnetic sensing, a comparator that amplifies the Hall Voltage, and a Schmitt trigger to provide switching hysteresis for noise rejection, open collector output. An internal band gap regulator is used to provide temperature compensated supply voltage for internal circuits and allows a wide operating supply range. The device is identical except for magnetic switch points.

A south pole of sufficient strength will turn the output on. The North Pole is necessary to turn the output off. An on-board regulator permits operation with supply voltages of 4V to 30 V.

The package type is in a Halogen Free version was verified by third party organization.

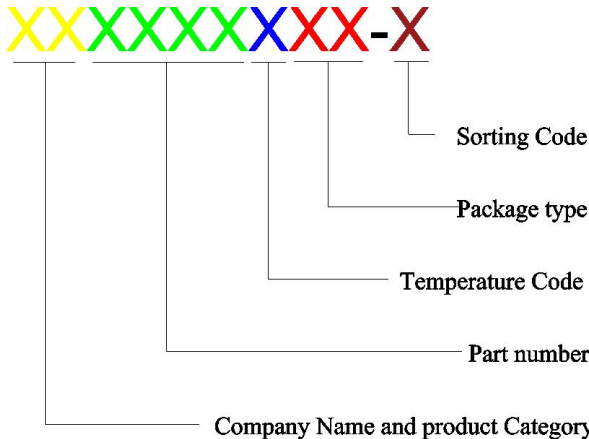
Features and Benefits

- Optimized for BLDC motor applications
- High Peak Voltage of 65V
- 100% tested at 125 °C for K.
- Temperature compensation function

Applications

- High temperature Fan motor
- 3 phase BLDC motor application
- Fan motor application
- Speed sensing
- Revolution counting
- E-Bike

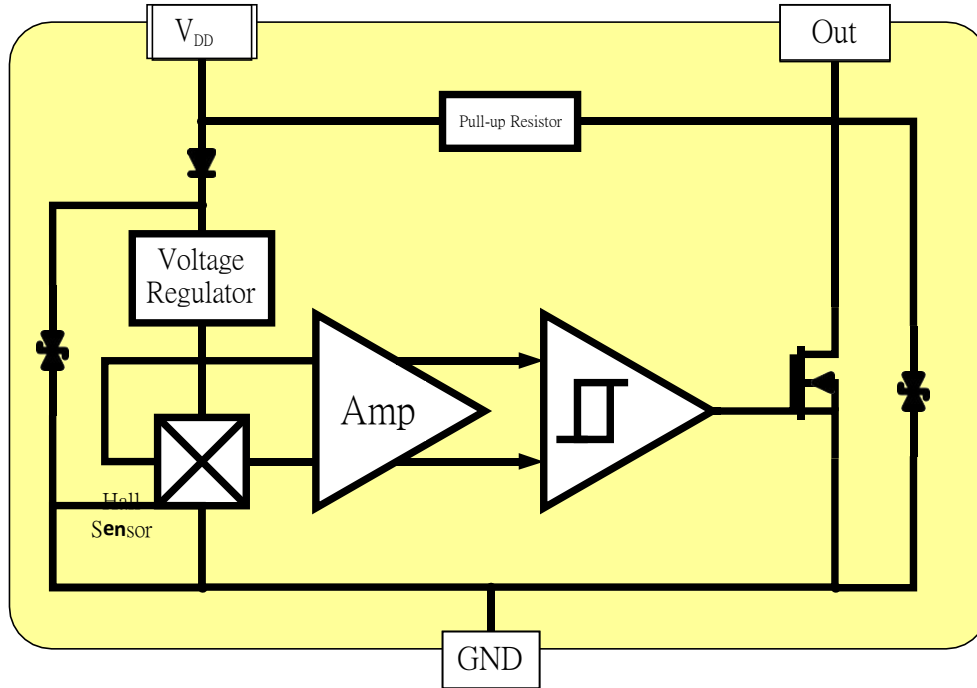
Ordering Information

	<p>Company Name and Product Category HH:HX Hall Effect/HP:HX Power IC</p> <p>Temperature range E: 85 °C, I: 105 °C, K: 125 °C, L: 150 °C</p> <p>Package type UA:TO-92S,VK:TO-92S(4pin),VF:TO-92S(5pin),SO:SOT-23, SQ:QFN-3,ST:TSOT-23,SN:SOT-553,SF:SOT-89(5pin), SS:TSOT-26,SD:DFN-6</p> <p>Sorting α,β,Blank.....</p>
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Part No.	Temperature Suffix	Package Type
HX6572KUA	K (-40°C to + 125°C)	UA (TO-92S)
HX6572KSO	K (-40°C to + 125°C)	SO (SOT-23)
HX6572EUA	E (-40°C to + 85°C)	UA (TO-92S)
HX6572ESO	E (-40°C to + 85°C)	SO (SOT-23)

KUA spec is using in industrial and automotive application. Special Hot Testing is utilized.

Functional Diagram



Absolute Maximum Ratings At ($T_a=25^\circ\text{C}$)

Characteristics		Values	Unit
Supply voltage, (V_{DD})		65	V
Output Voltage, (V_{out})		65	V
Reverse Voltage, (V_{DD}/V_{out})		-14/-0.3	V
Output current, (I_{SINK})		20	mA
Operating Temperature Range, (T_A)	“E” Class	-40 ~ +85	°C
	“K” Class	-40 ~ +125	°C
Storage temperature range, (T_S)		-65 ~ +150	°C
Maximum Junction Temp, (T_J)		150	°C
Thermal Resistance	(θ_{JA}) UA / SO	206 / 543	°C/W
	(θ_{JC}) UA / SO	148 / 410	°C/W
Package Power Dissipation, (P_D) UA / SO		606 / 230	mW

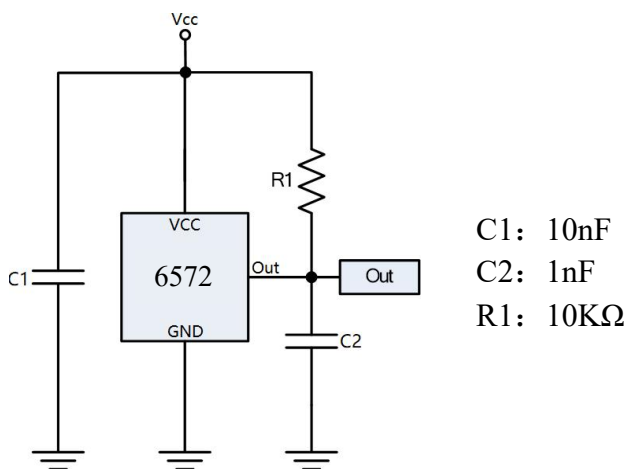
Note: Do not apply reverse voltage to V_{DD} and V_{OUT} Pin, It may be caused for Miss function or damaged device.

Electrical Specifications

DC Operating Parameters: $T_A = +25^\circ\text{C}$, $V_{DD} = 12\text{V}$

Parameters	Test Conditions	Min	Typ	Max	Units
Supply Voltage, (V_{CC})	Operating	4.0		30.0	V
Supply Current, (I_{CC})	$B < B_{OP}$		3.0	7.0	mA
Output Saturation Voltage, (V_{SAT})	$I_{OUT} = 5\text{mA}, B > B_{OP}$			500.0	mV
Output Leakage Current, (I_{off})	$I_{OFF} B < B_{RP}, V_{OUT} = 12\text{V}$			10.0	μA
Output Rise Time, (T_R)	$R_L = 820\Omega, C_L = 20\text{pF}$		1.5		μs
Output Fall Time, (T_F)	$R_L = 820\Omega; C_L = 20\text{pF}$		1.5		μs
Electro-Static Discharge	HBM(ACEQ-100)	4			KV

Typical application circuit



HX6572 Magnetic Specifications

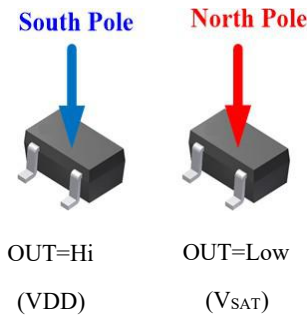
DC Operating Parameters: $T_A = +25^\circ\text{C}$, $V_{DD} = 12\text{V}$

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Operate Point	BOP	UA(SO)	10(-110)		110(-10)	Gauss
Release Point	BRP	UA(SO)	-110(10)		-10(110)	Gauss
Hysteresis	BHYS			100		Gauss

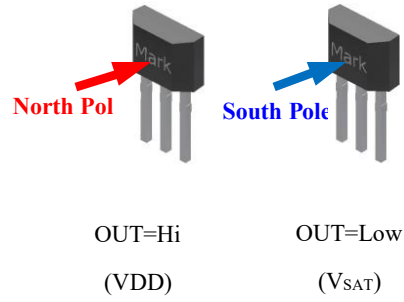
Output Behavior versus Magnetic Pole

DC Operating Parameters: $T_a = -40$ to 125°C , $V_{DD} = 4.0$ to 30V

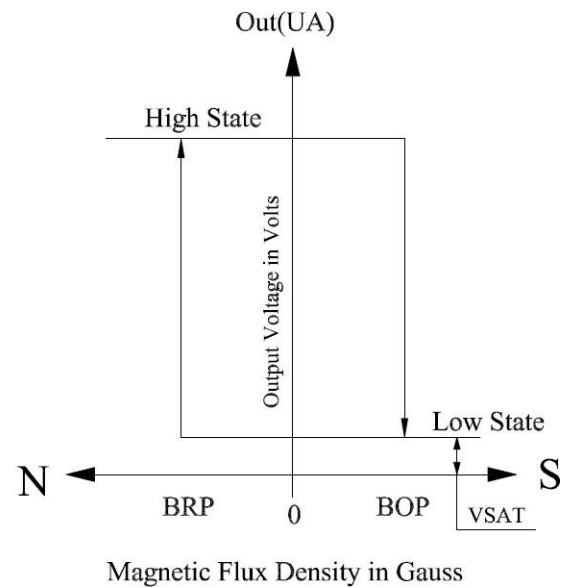
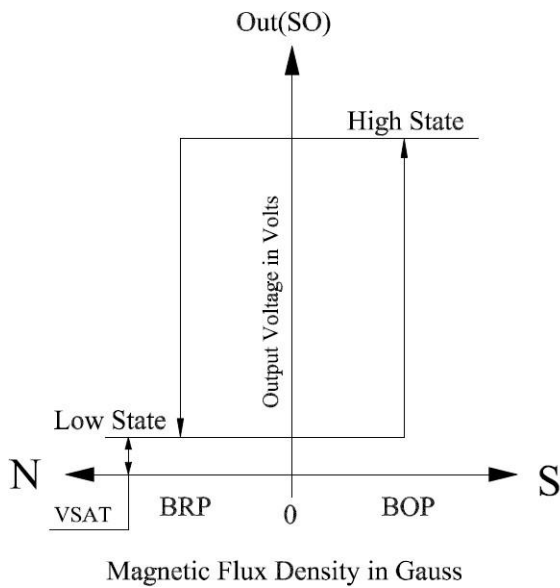
Parameter	Test condition	UA OUT	SO OUT
South pole	$B > B_{OP}$	Low(V_{SAT})	Open(Pull-up Voltage)
North pole	$B < B_{RP}$	Open(Pull-up Voltage)	Low(V_{SAT})



SO package

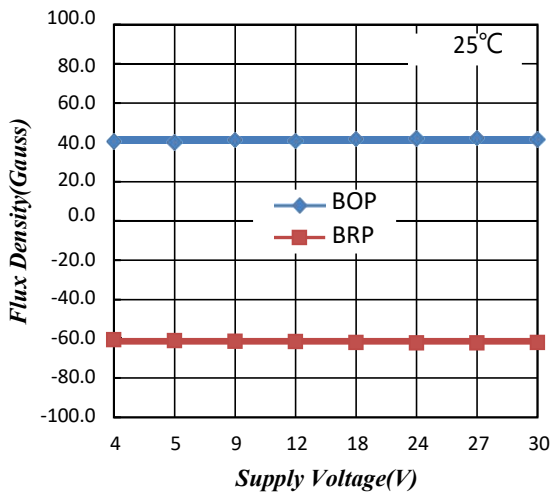


UA package

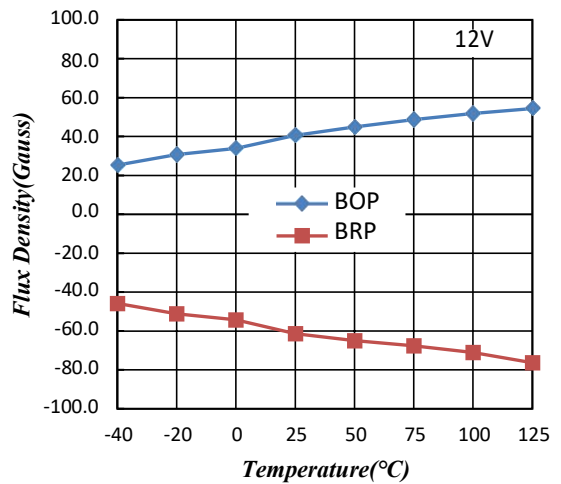


Performance Graph

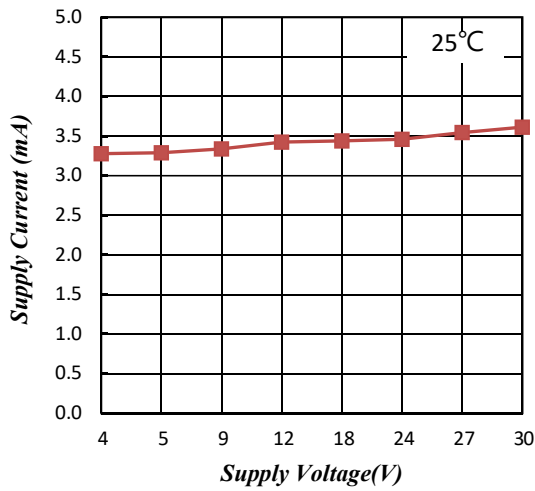
Typical Supply Voltage(V_{cc}) Versus Flux Density



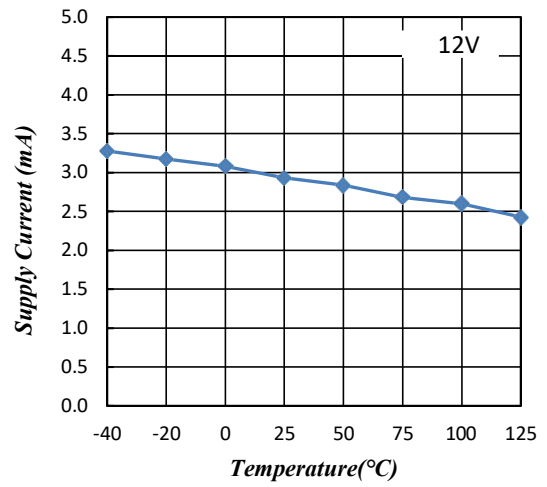
Typical Temperature(T_A) Versus Flux Density



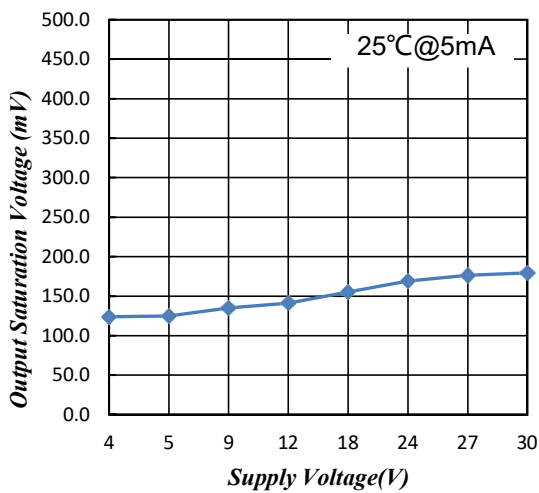
Typical Supply Voltage(V_{CC}) Versus Supply Current(I_{CC})



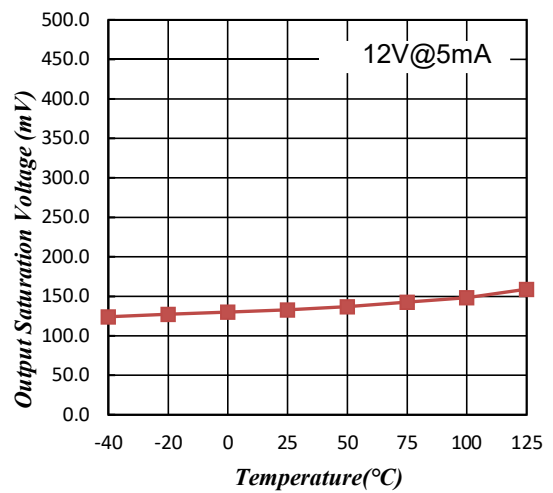
Typical Temperature(T_A) Versus Supply Current(I_{CC})



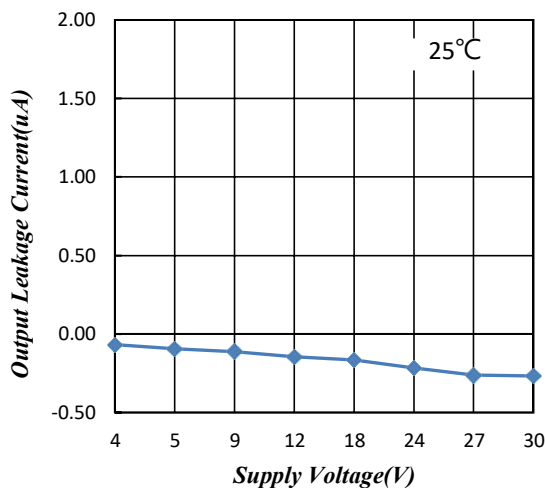
Typical Supply Voltage(V_{CC}) Versus Output Voltage(V_{SAT})



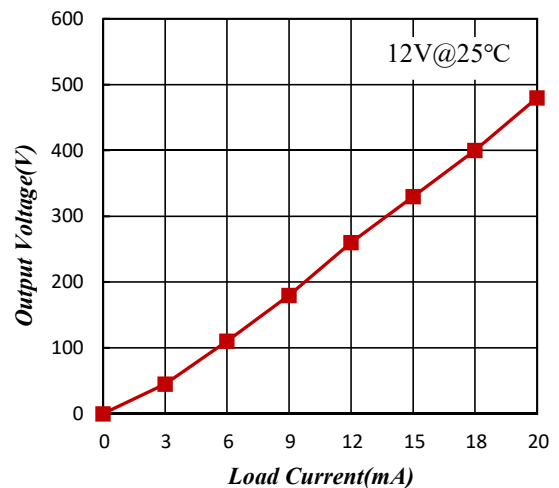
Typical Temperature(T_A) Versus Output Voltage(V_{SAT})



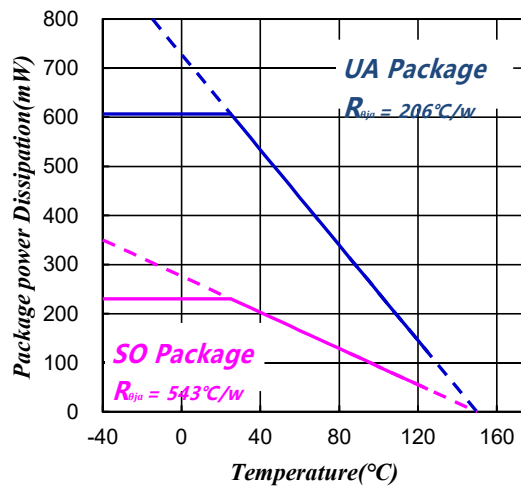
Typical Supply Voltage(V_{CC}) Versus Leakage Current(I_{OFF})



Typical Load Current(I_L) Versus Output Voltage(V_{OUT})



Power Dissipation versus Temperature(T_A)



Package Power Dissipation

The power dissipation of the Package is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_a . Using the values provided on the data sheet for the package, PD can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_a}{R_{\theta JA}}$$

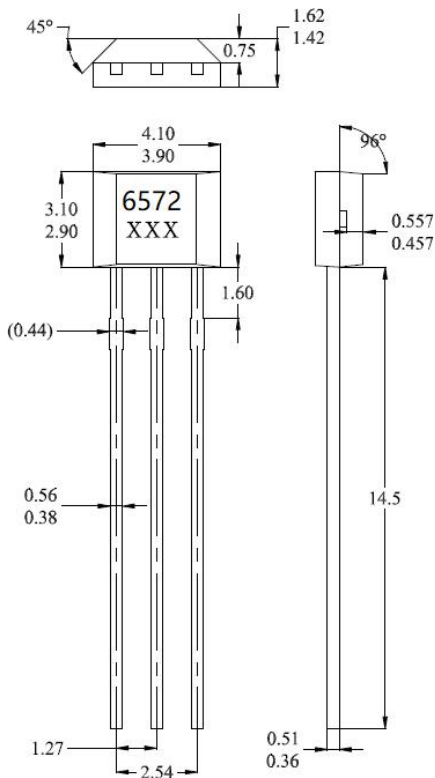
The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_a of 25°C, one can calculate the power dissipation of the device which in this case is 606 milliwatts.

$$P_D(UA) = \frac{150^\circ\text{C} - 25^\circ\text{C}}{206^\circ\text{C}/\text{W}} = 606\text{mW}$$

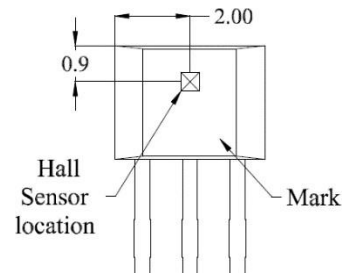
The 206°C/W for the UA package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 606 milliwatts. There are other alternatives to achieving higher power dissipation from the Package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

Sensor Location, Package Dimension and Marking

UA Package



Hall Chip location



NOTES:

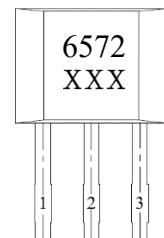
- 1).Controlling dimension: mm
- 2).Leads must be free of flash and plating voids
- 3).Do not bend leads within 1 mm of lead to package interface.

4).PINOUT:

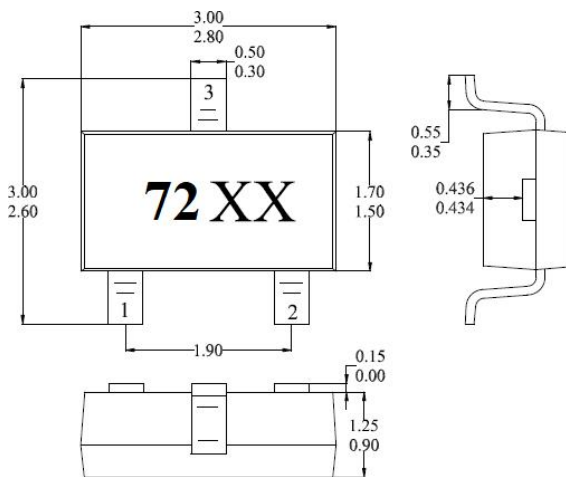
Pin 1	V _{DD}
Pin 2	GND
Pin 3	Output

Output Pin Assignment

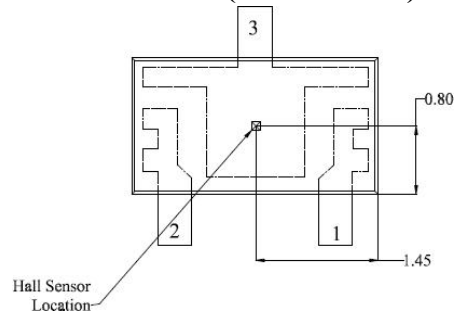
(Top view)



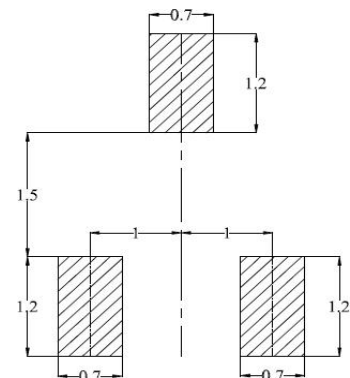
SO Package (Top View)



Hall Plate Chip Location (Bottom view)



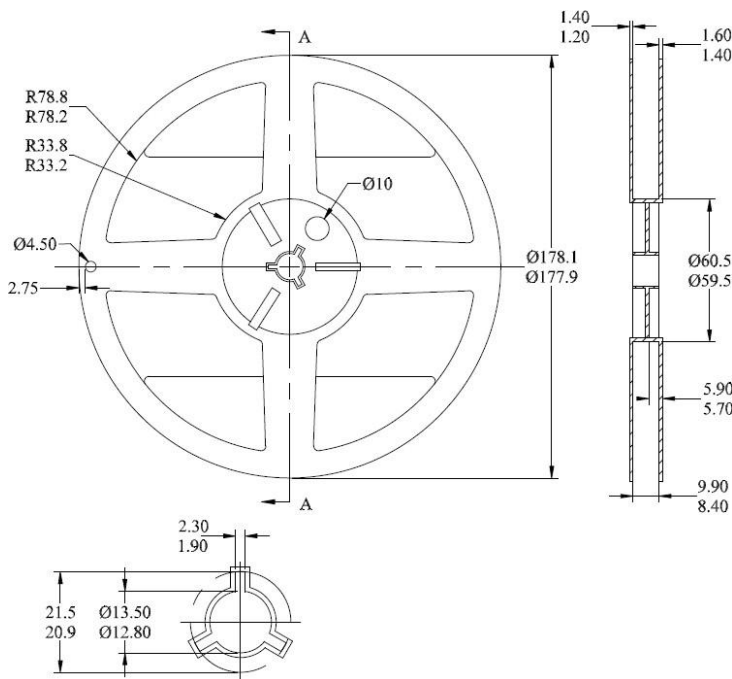
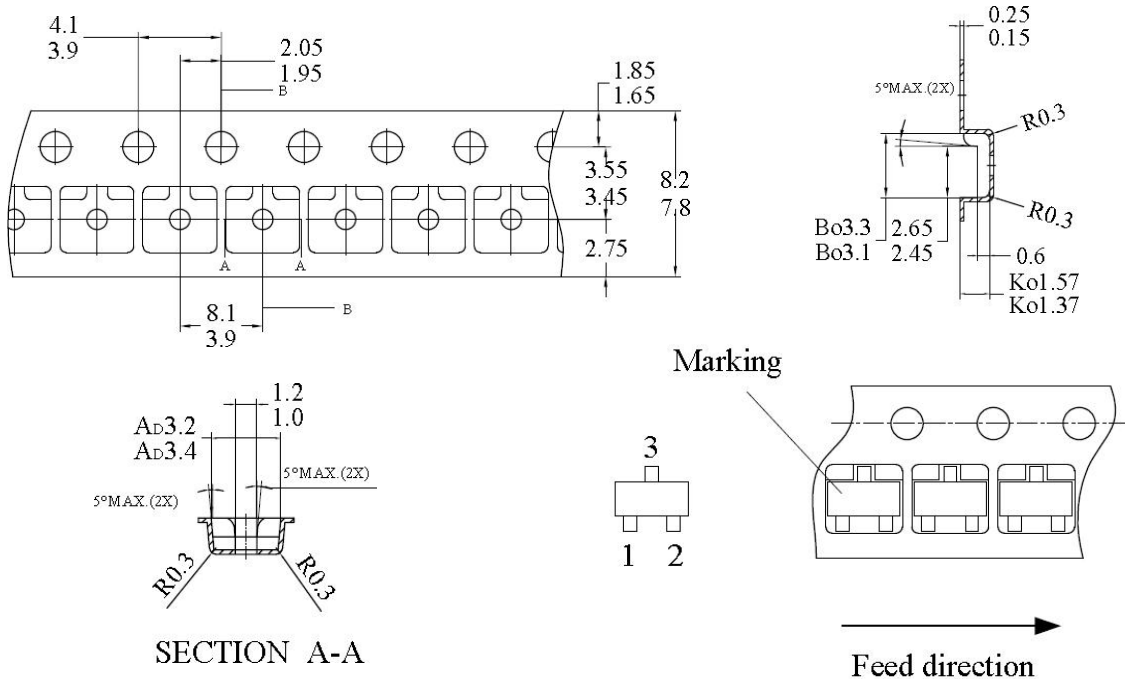
(For reference only) Land Pattern



NOTES:

1. PINOUT (See Top View at left :)
 - Pin 1 V_{DD}
 - Pin 2 Output
 - Pin 3 GND
2. Controlling dimension: mm
3. Lead thickness after solder plating will be 0.254mm maximum

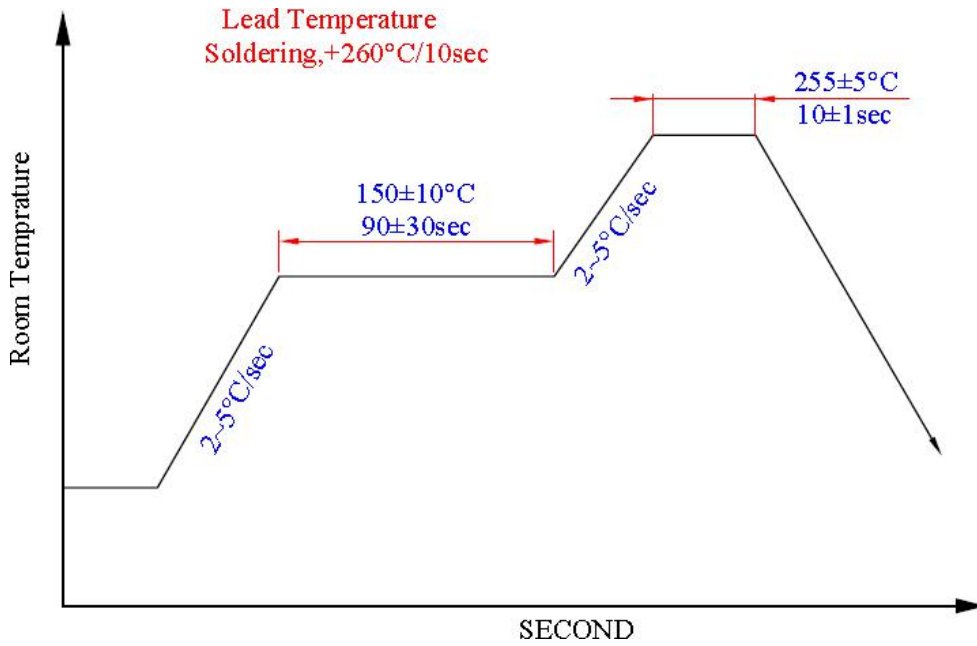
Sot-23 package Tape On Reel Dimension



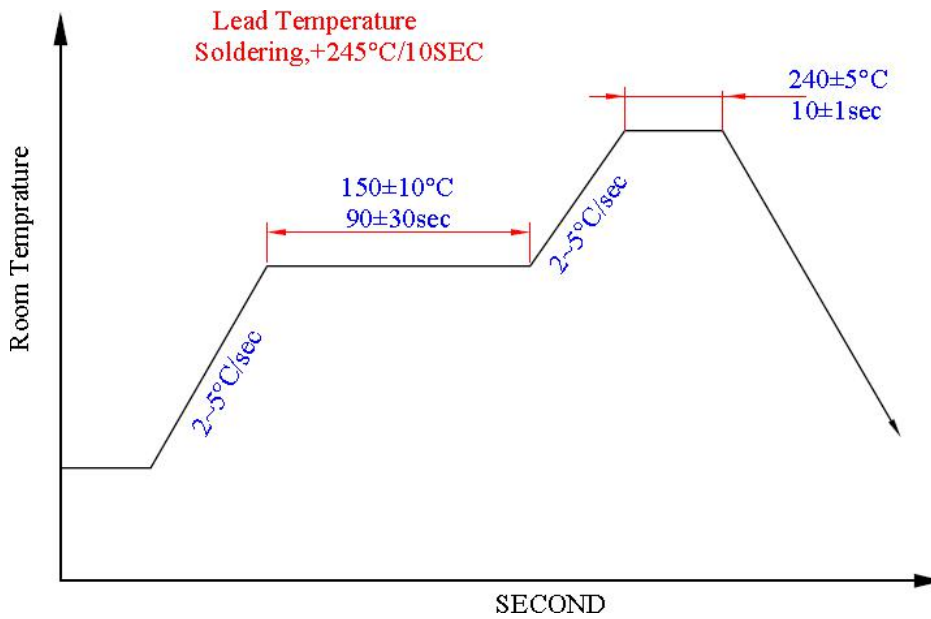
NOTES:

1. Material: Conductive polystyrene;
2. DIM in mm;
3. 10 sprocket hole pitch cumulative tolerance ± 0.2 ;
4. Camber not to exceed 1mm in 100mm;
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole;
6. (S.R. OHM/SQ) Means surface electric resistivity of the carrier tape.

IR reflow curve



SO Soldering Condition



UA Soldering Condition

Packing specification:

Package	Bag	Box	Carton	Carton	Carton
TO-92S-3L	1,000pcs/bag	10 bags/box	10 boxes/carton	5 boxes/carton	4 boxes/carton
SOT-23-3L	3,000pcs/reel	5 reels/box	6 boxes/carton	6 boxes/carton	6 boxes/carton

TO-92S-3L	Weight	SOT-23-3L	Weight
1000pcs/bag	0.11kg	3000pcs/reel	0.12kg
10 bags/box	1.26kg	5 reels/box	0.73kg
10 boxes/carton	13.38kg	6boxes/carton	4.84kg
5 boxes/carton	6.82kg	6boxes/carton	4.84kg
4 boxes/carton	5.54kg	6boxes/carton	4.84kg